What is claimed is:

1. A power-supply system capable of providing multiple operating functions to a computer, said power-supply comprising:

(a) a first DC power supply actuatable for providing a first operating function;

(b) cooling means coupled to said first DC power supply;

(c) a second DC power supply actuatable for providing a second operating function that does not require to activate said cooling means;

(d) a third DC power supply actuatable for providing a standby function to allow at least said first DC power supply when deactivated to be reactuatable for re-providing said first operating function;

(e) power output connector means connectable for respectively outputting said first DC power supply, said second DC power supply, and said third DC power supply; and

(f) control means for selectively activating said first DC power supply, said second DC power supply, and said third DC power to respectively provide said first operating function, said second operating function, and said standby function to said computer.

2. The computer power-supply system of claim 1 further comprising means for providing said first DC power supply, said second DC power supply, and said third DC power supply, wherein said means for providing is adapted to comprise at least one power provider selected from the group consisting of non-rechargeable battery, rechargeable battery, power-generating circuitry for generating DC power from AC power, and their combinations.

3. The computer power-supply system of claim 1 further comprising means for providing said first DC power supply, said second DC power supply, and said third DC power supply, wherein said power providing means is adapted to comprise power-generating circuitry for inputting AC power and for converting said AC power so as to selectively provide said first DC power supply, said second DC power supply, said third DC power supply, and their combinations.

4. The computer power-supply system of claim 1 further comprising a computer case for substantially enclosing said computer power-supply system and a manually-operable means disposed on the external side of said computer case for independently activating said second DC power supply.

5. The computer power-supply system of claim 1, wherein said cooling means is rendered temperature sensitive so as to be actuated only when the temperature of said computer power-supply system exceeds a preset value.

6. The computer power-supply system of claim 1, wherein said power output connector means is

adapted to comprise (i) a first connector means connectable with a computer motherboard for outputting at least said first DC power supply and said third DC power supply thereto; (ii) a plurality of second connector means coupled to said first DC power supply, each connectable for establishing power connection with a peripheral device in communication with said computer motherboard; and (iii) at least one third connector means each coupled to said first DC power supply and said second DC power supply; and wherein said control means is adapted to comprise (i) a first means signal-actuatable for deactivating both said first DC power supply and said second DC power supply to provide only said standby function to said first connector means and (ii) a second means manually-operable for activating said second DC power supply to provide only said second operating function to said at least one third connector means.

7. The computer power-supply system of claim 1, wherein said control means is adapted in a manner for selectively activating said first DC power supply, said second DC power supply, said third DC power supply, and their combinations.

8. The computer power-supply system of claim 1, wherein said control means is adapted in a manner selectively (i) for activating said first DC power supply, said second DC power supply and said third DC power supply at the same time to provide a full operating function, (ii) for activating said second DC power supply and said third DC power supply, but not for activating said first DC power supply to provide an energy-conserving operating function, (iii) for activating only said second DC power supply to provide an independent energy-conserving operating function, and (iv) for activating only said third DC power supply to provide said standby function.

9. The computer power-supply system of claim 1, wherein said control means is adapted in a manner for activating said second DC power supply at a condition selected from the group consisting of when said first DC power supply is activated or deactivated, when said third DC power supply is activated or deactivated, and their combinations, so as to allow a peripheral device coupled to said second DC power supply to be operable at any one of said conditions.

10. The computer power-supply system of claim 1, wherein said control means comprises a first switching means actuatable in response to a request signal for selectively activating or deactivating said first DC power supply and a second switching means manually-operable for selectively activating or deactivating said second DC power supply.

11. An energy-conserving motherboard having multiple operating functions, comprising:

(a) first power-distributing circuitry actuatable for providing a first operating function, wherein said first power-distributing circuitry is arranged for establishing power connection with main microprocessor circuitry;

(b) second power-distributing circuitry actuatable for providing a second operating function that does not require to activate said main microprocessor circuitry; and

(c) control means for selectively activating said first power-distributing circuitry and said second power-distributing circuitry, so as to respectively provide said first operating function and said second operating function.

12. The energy-conserving motherboard of claim 11, wherein said first power-distributing circuitry is arranged for establishing power connection further with means for cooling said main microprocessor circuitry.

13. The energy-conserving motherboard of claim 11, wherein said second power-distributing circuitry is arranged for establishing power connection with auxiliary microprocessor circuitry, random access memory circuitry, nonvolatile memory storage, and auxiliary video circuitry, so as to provide said second operating function for performing information processing without activating said first power-distributing circuitry.

14. The energy-conserving motherboard of claim 13, wherein said control means is adapted in a manner for activating said first power-distributing circuitry when detecting an activity of said auxiliary microprocessor circuitry is above a preset value.

15. The energy-conserving motherboard of claim 11, wherein said second power-distributing circuitry is arranged for establishing power connection with audio circuitry so as to provide said second operating function for producing audio information without activating said microprocessor circuitry.

16. The energy-conserving motherboard of claim 11 further comprising a third power-distributing circuitry for providing s standby function to allow both said first power-distributing circuitry and said second power-distributing circuitry to be deactivated, wherein said control means is adapted in a manner for firstly reactivating said second power-distributing circuitry to provide said second operating function when detecting a reactivating signal.

17. The energy-conserving motherboard of claim 11 further comprising third power-distributing circuitry for providing a standby function to allow at least said first power-distributing circuitry when deactivated to be reactuatable for re-providing at least said first operating function, wherein said third power-distributing circuitry is arranged for establishing power connection with standby circuitry for detecting a reactivating signal.

18. The energy-conserving motherboard of claim 17, wherein said third power-distributing circuitry is arranged for establishing power connection further with keep-alive memory circuitry for storing information needed for resuming activities associated with said first operating function.

19. The energy-conserving motherboard of claim 17, wherein said control means is adapted in a manner for activating said second power-distributing circuitry at a condition selected from the group consisting of when said first power-distributing circuitry is activated or deactivated, when said third power-distributing circuitry is activated or deactivated, and their combinations.

20. The energy-conserving motherboard of claim 17, wherein said control means is adapted in a manner for selectively (i) activating said first power-distributing circuitry and said second power-distributing circuitry at the same time to provide a full operating function, (ii) activating said second power-distributing circuitry and said third power-distributing circuitry without activating said first power-distributing circuitry to provide an energy-conserving operating function, (iii) activating only said second power-distributing circuitry to provide an independent energy-conserving operating function, and (iv) activating only said third power-distributing circuitry to provide only said standby function.

21. The energy-conserving motherboard of claim 11, wherein said control means is adapted in a manner for deactivating said first power-distributing circuitry when detecting an activity of said main microprocessor circuitry is below a preset value.

22. The energy-conserving motherboard of claim 11, wherein said control means comprises a first means actuatable in response to a signal for selectively activating or deactivating said first power-distributing circuitry and a second means manually-operable for selectively activating or deactivating said second power-distributing circuitry.

23. An information-processing apparatus having multiple operating functions, comprising:

(a) a first group of circuitry actuatable for providing a first operating function, wherein said first group of circuitry comprises main microprocessor circuitry;

(b) a second group of circuitry actuatable for providing a second operating function that does not require to activate said main microprocessor circuitry;

(c) a third group of circuitry actuatable for providing a standby function to allow at least said first group of circuitry when deactivated to be reactuatable for providing said first operating function;

(d) power providing means for providing power at least to said first group of circuitry, said second group of circuitry, and said third group of circuitry; and

(e) control means for controlling said power providing means to selectively activate said first group of circuitry, said second group of circuitry, and said third group of circuitry, so as to respectively provide said first operating function, said second operating function, and said standby function.

24. The information-processing apparatus of claim 23, wherein said first group of circuitry further comprises means for cooling said main microprocessor circuitry.

25. The information-processing apparatus of claim 23, wherein said second group of circuitry comprises audio circuitry, so as to provide said second operating function for producing audio information without activating said main microprocessor circuitry.

26. The information-processing apparatus of claim 23, wherein said second group of circuitry comprises auxiliary microprocessor circuitry, volatile memory storage, nonvolatile memory storage, and auxiliary video circuitry, so as to provide said second operating function for performing information processing without activating said main microprocessor circuitry.

27. The information-processing apparatus of claim 26, wherein said nonvolatile memory storage is selected from the group consisting of battery-powered random-access memory, at least one hard-disk drive, at least one optical disc drive, and their combinations.

28. The information-processing apparatus of claim 26, wherein said control means is adapted for controlling said power providing means to activate said first group of circuitry when detecting an activity of said auxiliary microprocessor circuitry is above a preset value.

29. The information-processing apparatus of claim 23, wherein said third group of circuitry comprises standby circuitry including (i) keep-alive random access memory for storing task information to be reactivated and (ii) control circuitry responsive to a reactivating signal for restoring said task information, so as to provide said standby function for deactivating and reactivating said task information.

30. The information-processing apparatus of claim 23, wherein said third group of circuitry is adapted to comprise keep-alive random access memory for storing task information to be reactivated and said control means is adapted to comprise standby circuitry responsive to a reactivating signal for restoring said task information, so as to provide said standby function for deactivating and reactivating said task information respectively associated with said first operating function and said second operating function.

31. The information-processing apparatus of claim 23, wherein said power providing means comprises at least one power provider selected from the group consisting of non-rechargeable battery, rechargeable battery, power circuitry for generating DC power from AC power, and their combinations, for providing a first DC power supply, a second DC power supply, a third DC power supply, and their power combinations respectively to said first group of circuitry, said second group of circuitry, said third group of circuitry, and their group combinations.

32. The information-processing apparatus of claim 23, wherein said power providing means is adapted to comprise power circuitry for inputting AC power and for converting said AC power selectively

to a first DC power supply, a second DC power supply, a third DC power supply, and their power combinations respectively to said first group of circuitry, said second group of circuitry, said third group of circuitry, and their group combinations.

33. The information-processing apparatus of claim 23, wherein said power providing means comprises rechargeable battery and said control means is adapted for controlling said rechargeable battery not to energize said first group of circuitry when detecting an activity of said main microprocessor circuitry is below a preset value, so as to conserve the power of said rechargeable battery.

34. The information-processing apparatus of claim 23, wherein said control means is arranged to have power connection with said third group of circuitry so as to be energized for controlling said power providing means to selectively reactivate said first group of circuitry and said second group of circuitry, when said standby function is provided.

35. The information-processing apparatus of claim 23, wherein said control means is adapted for controlling said power providing means to deactivate said first group of circuitry when detecting an activity of said main microprocessor circuitry is below a preset value.

36. The information-processing apparatus of claim 23, wherein said control means is adapted selectively (i) for activating at least said first group of circuitry and said second group of circuitry at the same time to provide a full operating function, (ii) for activating said second group of circuitry and said third group of circuitry without activating said first group of circuitry to provide an energy-conserving operating function, (iii) for activating only said second group of circuitry to provide an independent energy-conserving operating function, and (iv) for activating only said third group of circuitry to provide said standby function.

37. The information-processing apparatus of claim 23, wherein said control means comprises (i) a first means actuatable in response to a signal for controlling said power providing means to selectively activate or deactivate said first group of circuitry, and (ii) a second means manually-operable for controlling said power providing means to selectively activate or deactivate said second group of circuitry.

38. The information-processing apparatus of claim 23 further comprising a central processor unit that comprises said main microprocessor circuitry comprised in said first group of circuitry and auxiliary microprocessor circuitry comprised in said second group of circuitry.

39. The information-processing apparatus of claim 23 further comprising an optical disc drive and a fourth group of circuitry arranged for providing an audio-reproduction function at a condition when said first group of circuitry, said second group of circuitry, and said third group of circuitry are all deactivated.

40. The information-processing apparatus of claim 23 further comprising at least two optical disc

drives and a fourth group of circuitry arranged for providing a read and write function therebetween at a condition when said first group of circuitry, said second group of circuitry, and said third group of circuitry are all deactivated.

41. The information-processing apparatus of claim 23 further comprising (i) a motherboard for disposing said first group of circuitry, said second group of circuitry, and said third group of circuitry, (ii) an optical disc drive having power connection with said second group of circuitry, and (iii) audio circuitry comprised in said second group of circuitry, so as to provide said second operating function for producing audio information even at a condition when said first group of circuitry and said third group of circuitry are both deactivated.

42. An operating system for controlling an activity of an information-processing apparatus having main microprocessor circuitry and auxiliary microprocessor circuitry, said operating system comprising the instructions of:

(a) monitoring an activity of said main microprocessor circuitry;

(b) comparing said activity with a preset value;

(c) deactivating said main microprocessor circuitry, if said activity has a value smaller than said preset value; and

(d) deactivating said auxiliary microprocessor circuitry, if said activity has a value of zero.

43. The operating system of claim 42, wherein said instructions are stored on a random access memory chip.

44. The operating system of claim 42 further comprising an additional instruction for activating said auxiliary microprocessor circuitry if said activity has a value greater than zero but smaller than said preset value.

45. The operating system of claim 42 further comprising an additional instruction for saving any modified files to nonvolatile memory storage, when deactivating said auxiliary microprocessor circuitry.

46. The operating system of claim 42 further comprising an additional instruction for saving the activities of said information-processing apparatus to keep-alive random access memory if to request said deactivating.

47. The operating system of claim 42 further comprising an additional instruction for activating said main microprocessor circuitry if detecting a request signal.

48. An operating system for controlling an activity of an information-processing apparatus having main microprocessor circuitry and auxiliary microprocessor circuitry, said operating system comprising the instructions of:

(a) monitoring an activity of said auxiliary microprocessor circuitry;

(b) comparing said activity with a preset value; and

(c) activating said main microprocessor circuitry, if said activity has a value greater than said preset value.

49. The operating system of claim 48, wherein said instructions are stored on a random access memory chip.

50. The operating system of claim 48 further comprising an additional instruction for activating said main microprocessor circuitry only if said activity has a time value greater than a preset time value.

51. The operating system of claim 48 further comprising an additional instruction for deactivating said main microprocessor circuitry if said activity has a value not greater than said preset value, wherein said preset value is greater than zero.

52. The operating system of claim 48 further comprising an additional instruction for deactivating said auxiliary microprocessor circuitry if said activity has a value of zero.

53. The operating system of claim 52 further comprising an additional instruction for saving the activities of said information-processing apparatus to keep-alive random access memory if to request said deactivating.

54. The operating system of claim 52 further comprising an additional instruction for activating said main microprocessor circuitry if detecting a request signal.